ELECTRONIC INFORMATION DISCLOSURE STATEMENT

Electronic Version v18

Stylesheet Version v18.0

Title of Invention

THE USE OF A LAYOUT-OPTIMIZATION TOOL TO INCREASE THE YIELD AND RELIABILITY OF VLSI DESIGNS

Application Number:

Confirmation Number:

First Named Applicant:

Robert Allen

Attorney Docket Number:

BUR920030092US1

Art Unit:

Examiner:

Search string:

(4831725 or 5459690 or 5796274 or 5798937 or 6026224 or 6189132 or 6484301

or 6556658).pn

US Patent Documents

Note: Applicant is not required to submit a paper copy of cited US Patent Documents

init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass	
mu	1	4831725	1989-05-23	Dunham et al.				
mu	, 2	5459690	1995-10-17	Rieger et al.	-		-	
mi	/ 3	5796274	1998-08-18	Willis et al.				
Mu	4	5798937	1998-08-25	Bracha et al.				
MU	5	6026224	2000-02-15	Darden et al.				
Mu	6	6189132	2001-02-13	Heng et al.				
MU	7	6484301	2002-11-19	Burden				
MW	8	6556658	2003-04-29	Brennan				

Signature

Date
3/2005

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INFORMATION DISCLOSURE CITATION (Use several sheets if necessary)				ATTY DOCKET NO. BUR920030092US1		SERIAL NO. Not Yet Assigned			
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mw	Chen et al., "Layout Tec Optical Engineering Cor	hniques for VLSI \ nference", vol. 4600	Yield Enhancement", Proceedi 0, 2001, pp. 140-147.	ngs of the SPIE -	The Internati	onal Society	y for		
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